Archit Bhatnagar

architb@umich.edu | archit-bhatnagar.github.io | archit-bhatnagar | Archit Bhatnagar

Education

University of Michigan, Ann Arbor
Ann Arbor

PhD, Computer Science — *Aug. 2024*

Advised by: Prof. Ang Chen

Birla Institute of Technology and Science(BITS), Pilani
Pilani,India

B.E. Computer Science — *Aug. 2019 - June 2023*

- **Thesis**: Secure-In-Band-communication-using-Programmable-switches. *National University of Singapore*
- **Cumulative GPA**- 8.68/10
- **Relevant Courses:** Adv. Computer Networks, Computer Architecture, Compiler Construction, IoT, Operating Systems

Publications

P4EAD: Securing the In-band Control Channels on Commodity Programmable Switches [Paper] [Code]
Archit Bhatnagar*, Xin Zhe Khooi*, Cha Hwan Song, Mun Choon Chan
Proceedings of the 6th European P4 Workshop (EuroP4 '23), 2023

Poster: **Towards Accelerating the 5G Centralized Unit with Programmable Switches** [Paper] [Poster]
Xin Zhe Khooi, **Archit Bhatnagar**, Satis Kumar Permal, Nishant Budhdev, Cha Hwan Song, Mun Choon Chan
Proceedings of the ACM SIGCOMM 2023 Conference, 2023

Technical Skills

Programming/Scripting C/C++, Python, MATLAB, Verilog, Git, Bash | **Tools:** Mininet, Scapy, ns-3
Programmable Networking **Data Plane:** $P4_{16}$ | **Arch:** V1Model, TNA | **Control Plane:** BfRt, OpenFlow, POX
ML/DL Libraries TensorFlow, OpenCV, Mediapipe, Sklearn

Research & Work Experience

Systems & Networking Lab, NUS
Singapore

Research Assistant, Supervisor: Prof. Ben Leong — *Sept 2023 - June 2024*

- Working with **ns-3** and **P4** to implement and validate a novel queuing mechanism for ensuring bounded unfairness.
- Implementing and verifying components for a **P4Campus**-like infrastructure for **Internet measurements** at the NUS School of Computing.

Communication and Internet Research Lab, NUS
Singapore

Research Intern, Supervisor: Prof. Chan Mun Choon — *Jan 2023 - July 2023*

- Worked on securing **in-band control channels** on programmable switches implementing **authenticated encryption**.
- Offloaded core **5G CU** functionalities on a Tofino switch, improving the median latency by **80 times**.

Samsung Research
Delhi,India

Intern — *June 2022 - July 2022*

- Worked on integration of temporally encoded video formats(H.264) in **USB Video Class**(UVC) 1.1.
- Analyzed UVC 1.1 and 1.5 revisions, adapted the **extension unit** for dependency on **stream-based** payload formats.

LiveSmart
Remote

Research Intern, Supervisor: Prof. Kamlesh Tiwari — *February 2022 - May 2022*

- Developed a vision-based model to detect **joint mobility** problems among seniors using **gait recognition**.
- Reviewed and designed motion characteristics to help detect joint mobility problems with a **96%** accuracy.

CEERI-CSIR, Chennai

Chennai,India

Research Intern *June 2021 - July 2021*

- Implemented **Local Binary Patterns** (CLBP & MRELBP) using Tensorflow for **texture classification**.
- Improved accuracy by 5%(86 to 91%) using Deep Learning architectures like **Bilinear CNNs** and AlexNet.

Projects

P4EAD: Securing in-band control channel on prog. switches

$P4_{16}$, Intel Tofino P4 Studio, BfRt, Scapy

- Implemented ASCON cipher-suite based authenticated encryption using **$P4_{16}$** on Intel **Tofino** switches.
- Further optimized throughput by **2x**, benchmarked the performance authenticating packets at multi-Gbps rates.

ML-based Relay Selection for Co-op mmWave Communication

MATLAB, Wireless Communication, ML

- Designed and compared **relay selection** policies in a dual-hop setup for cooperative **mmWave communication** (5G).
- Optimized **energy & spectral efficiency** by **6dB**, feeding the compiled **CSI** to a probabilistic model and a neural network.

PoseMatchNet

Python, TensorFlow, OpenCV

- Designed an efficient **siamese architecture** to **compare complex poses** performed by people using RGB images.
- Improved the model for **robustness** in challenges related to occlusion, inter-class similarity & viewpoint complexity.

Course Projects

Compiler Design - Compiler in C

C, Low-Level Programming

- Designed a custom compiler in C supporting **assignment, i/o, iterative, conditional** statements and function calls.
- Implemented the Lexical, Semantic & Syntactic Analyzer, Parser and **Abstract Syntax Tree(AST)**.

Hybrid FlowSense for Network Monitoring

Mininet, POX, SDN

- Implemented FlowSense for **passive network monitoring** with control messages using **Mininet** & **POX** Controller
- Added **active probing** based on **flow-specific timers** and counters for granular monitoring with low overhead.

Teaching Experience

Teaching Assistant *Sept 2022- Dec 2022*

- Teaching Assistant for undergraduate course CS F432-**Computer Architecture** with around 250 students.
- Conducting **weekly lab sessions** in Verilog-HDL for the course under Dr. Sudeept Mohan

Scholarships Awarded

2023 **BITS Pilani International Program and Collaboration Division financial aid**, for doing an off-campus Bachelor's thesis at NUS. *Pilani, India*

2019 **HScTSS (Haryana Science Talent Search Scheme)**, Rs.36,000 for NTSE Stage -1,by SCERT Haryana *Haryana, India*

Achievements

- JEE (Mains)-Obtained a rank of **5389 among 1.2 million** students(**top 0.5 %ile**) who appeared for the test in 2019
- CBSE Board Examinations- Obtained **95.8% marks** in the Science Stream(with Computer Science), was in the **top 0.1 %ile among 1.3 million** students in 2019.