# Archit Bhatnagar

(+91) 8826227510 | f20190133@pilani.bits-pilani.ac.in | archit-bhatnagar.github.io | archit-bhatnagar

## Education

### Birla Institute of Technology and Science(BITS),Pilani

*Pilani,India*

B.E.(Hons.) Computer Science — *Aug. 2019 - June 2023*

- **Cumulative GPA**- 8.68/10
- **Relevant Courses:** Adv. Computer Networks, IoT, Computer Architecture, Compiler Construction, Neural Networks & Fuzzy Logic, Digital Design, Operating Systems, Data Structures and Algorithms, Object Oriented Programming, Database Management Systems, Probability & Stats, Linear Algebra

## Technical Skills

| | |
|---|---|
| **Programming/Scripting** | C/C++, Python, MATLAB, Java, Verilog, Git, Bash \| **Tools:** Mininet, Scapy, ns-2 |
| **Programmable Networking** | **Data Plane:** $P4_{16}$ \| **Arch:** V1Model, TNA \| **Control Plane:** BfRt, OpenFlow, POX |
| **Python ML Libraries** | TensorFlow,OpenCV,Mediapipe,Sklearn |

## Research & Work Experience

### Systems & Networking Lab, NUS

*Singapore*

Research Intern — *Jan 2023 - June 2023*

- Worked on **securing in-band control channels** on **programmable switches** utilizing **ASCON** cipher-suite.
- Implemented **authenticated encryption** at multi-Tbps line-rates using **P4** programs on **Intel Tofino** switches.
- Reviewing congestion control and **TCP-ack pacing** for **wireless** networks on programmable switches.

### Samsung Research

*Delhi,India*

Intern — *June 2022 - July 2022*

- Worked on integration of temporary **video class** formats **(H.264)** in **USB Video Class**(UVC) 1.1.
- Analyzed key differences between **UVC 1.1 and 1.5** revisions in regards to support for **video controllers** and **USB 3.0**.
- Adapted the **extension unit** to adjust dependence on **stream-based payload** formats as a part of Device Solutions Group .

### LiveSmart

*Remote*

Research Intern, Supervisor: Dr. Kamlesh Tiwari — *February 2022 - May 2022*

- Developed a vision-based model to detect **joint mobility** problems among seniors using **gait recognition**.
- Designed an interface to **graphically analyze** the **walking patterns** and mobility between the joints in real time.
- Reviewed and designed new features to help detect joint mobility problems with a **96%** accuracy.

### CEERI-CSIR, Chennai

*Chennai,India*

Research Intern — *June 2021 - July 2021*

- Implemented **Local Binary Patterns** (CLBP & MRELBP) using Tensorflow for **texture classification**.
- Classified the LBP vectors using **KNN, SVM**, decision trees & logistic regression with **varying resolutions**.
- Improved accuracy by **5%**( 86 to 91%) using Deep Learning architectures like **Bilinear CNNs** and AlexNet.

## Projects

### P4EAD: Securing in-band control channel on prog. switches

$P4_{16}$, Intel Tofino P4 Studio, BfRt, Scapy

- Implemented ASCON cipher-suite based authenticated encryption using **$P4_{16}$** on Intel **Tofino hardware** switches.
- Optimized the implementation further to **double** the **throughput** using in_hash pragma for complex operations.
- Benchmarked the performance of P4EAD by **generating packets** at multi-Gbps rates **gRPC** on Tofino hardware switches.

### ML-based Relay Selection for Co-op mmWave Communication

MATLAB, Wireless Communication, ML

- Designed and compared **Relay Selection** policies in a Dual-hop setup for cooperative **mmWave Communication** (5G).
- Optimized **Energy & Spectral Efficiency** by **6dB**, feeding the compiled **CSI** to a probabilistic model and a neural network.

### PoseMatchNet

Python, TensorFlow, OpenCV

- Designed an efficient **siamese architecture** to **compare complex poses** performed by people using RGB images.
- Compared variations like multi-level perceptron, **affine transforms** & siamese networks,in terms of **accuracy vs latency**.
- Improved the model for **robustness** in challenges related to **occlusion**, inter-class similarity, **viewpoint complexity**,etc.

## Course Projects

### Compiler Design - Compiler in C

C, Low-Level Programming

- Designed a custom compiler in C supporting **assignment, i/o, iterative, conditional** statements and function calls.
- Included functionalities like **returning multiple values** from a function, **recursion & static scoping** of variables.
- Implemented the **Lexical, Semantic & Syntactic Analyzer, Parser** and **Abstract Syntax Tree(AST)**.
- Obtained the intermediate **3 address codes** from AST, converted them to **machine code** & executed it using **NASM**.

### Hybrid FlowSense for Network Monitoring

Mininet, POX, SDN

- Implemented FlowSense for **passive network utilization** monitoring for each flow with control messages.
- Used **POX** Controller to evaluate Flowsense on a custom **Mininet** topology with an Iperf UDP flow.
- Added **active probing** based on **flow-specific timers** and byte **counters** for granular utilization monitoring with low additional overhead.

### River Pollution Monitoring using ESP8266

ESPnow, React

- Implemented a proof of concept for **real-time** water pollution monitoring using **2 ESP8266 modules** interfaced with **DHT-11 sensors**, with one node acting as the master.
- Used **ESPnow MAC** protocol for inter-node connection **simultaneously** with the master node to firebase communication.
- Designed a webpage using **React**, to display the real-time DHT sensor readings & hosted it on a **Flask** development server.

### Floating Point Divider

Verilog HDL

- Implemented a **32 bit floating point divider** for single precision floating point numbers defined **IEEE 754**.
- Used **Verilog HDL** for designing modules based on **iterative subtraction for division**,handling multiple edge cases.
- Built robust modules capable of handling **invalid operations and overflows**, implemented a **testbench** to validate it.

## Teaching Experience

Teaching Assistant — *Sept 2022- Dec 2022*

- Teaching Assistant for undergraduate course CS F432-**Computer Architecture** with around 250 students.
- Conducting **weekly lab sessions** in Verilog-HDL for the course under Dr. Sudeept Mohan

## Scholarships Awarded

2019 **HScTSS (Haryana Science Talent Search Scheme)**, Rs.36,000 for NTSE Stage -1,by SCERT Haryana — *Haryana, India*

## Achievements

- JEE (Mains)-Obtained a rank of **5389 among 1.2 million** students(**top 0.5 %ile**) who appeared for the test in 2019
- CBSE Board Examinations- Obtained **95.8% marks** in the Science Stream( with Computer Science), was in the **top 0.1 %ile among 1.3 million** students in 2019.